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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,576	04/21/2004	Shawn X. Du	130567/GLOZ200129	5300

27885 7590 04/15/2008
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EXAMINER	
ARENA, ANDREW OWENS	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
04/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,576	DU ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,18,23 and 26-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6, 18, 23 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

Claims 4-6 are rejected under 35 U.S.C. § 102(e) as being anticipated by Camras (US 6,784,463).

RE claim 5, Camras discloses a method of manufacturing a light emitting diode (col 3 ln 55-60, col 4 ln 9-12), the method comprising (e.g., Figs 4 & 6, col 11 ln 21-24):

depositing (Fig 6A) a plurality of semiconductor layers (112, 114, 116) on a deposition substrate (140, col 11 ln 25, col 10 ln 25-40);

removing (Fig 6D) at least some of the deposited semiconductor layers from a selected trench region of the deposition substrate to define a light-emissive mesa (110 in Fig 5D, col 11 ln 36-40);

forming an electrode (118, col 11 ln 38) on the mesa;

flip-chip bonding (Fig 4, col 9 ln 30-32) the mesa to a first electrical bonding pad (134) of a thermally conductive (to any extent, as per MPEP § 2111) support (130);

removing the deposition substrate (col 11 ln 27); and

subsequent to the removing of the deposition substrate, non-epitaxially depositing (col 10 ln 41-46) a light-transmissive, electrically conductive (transparent semiconductor: col 4 ln 64-65) window layer (117) on a surface of the mesa opposite the electrode, the window layer extending laterally to electrically contact a second electrical bonding pad (138) of the thermally conductive support to define an electrical path between the mesa and the second electrical bonding pad (col 8 ln 12-23).

RE claim 4, Camras discloses depositing said semiconductor layers by a deposition technique selected from the group consisting of metalorganic chemical vapor deposition and molecular beam epitaxy (col 10 ln 27-34, col 11 ln 23-26).

RE claim 6, Camras discloses the removing of the deposition substrate effects a physical separation of the mesa wherein mesa defines a separated light emitting diode device die flip-chip bonded to the thermally conductive support (Fig 4; col 11 ln 62-65).

Claim Rejections - 35 USC § 103

Claim 3 is rejected under 35 U.S.C. § 103(a) as being obvious in view of Camras as applied to claims 5 above, further in view of Shieh (US 5,780,321).

RE claim 3, Camras differs from the claimed invention only in not expressly disclosing an insulating material between the second bonding pad and the mesa.

Shieh discloses (e.g., Fig 2) prior to removal of the substrate (12, Fig 4-Fig 5), depositing an insulating layer (clear portions on sides of mesa must insulate) at least on sidewalls of the mesa.

Camras discloses deposition of the window layer and bonding to the bonding pads after removal of the substrate (col 11 ln 27-29).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Shieh, the method of Camras include prior to the depositing of a window layer, depositing an insulating material on at least sidewalls of the mesa and between the second electrical bonding pad and the mesa, the window layer extending laterally over the insulating material; at least to prevent possible shorts.

Claims 18, 23 and 26-31 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Camras and Goosen (US 5,923,951).

RE claim 18, Camras discloses a method of manufacturing a flip-chip (col 9 ln 30-32) light emitting diode (col 3 ln 55-60, col 4 ln 9-12), the method including (e.g., Figs 4 & 6, col 11 ln 21-24):

epitaxially depositing (Fig 6A; col 10 ln 27-34, col 11 ln 23-25) semiconductor layers (112, 114, 116) that define a light emitting electrical junction on a principle surface of an epitaxy substrate (140);

forming (Fig 6D) a light-emitting device mesa (110 in Fig 5D; col 11 ln 36-40) from the epitaxially deposited semiconductor layers;

forming a first electrode (118, col 11 ln 38) on a portion of the device mesa distal from the epitaxy substrate, the first electrode electrically contacting the device mesa;

disposing a second electrode (120) on the principle surface of the substrate;

flip-chip bonding (Fig 4, col 9 ln 30-32) first and second electrodes to bonding pads (134, 138; col 9 ln 35-39);

removing the epitaxy substrate (col 11 ln 27); and

subsequent to the removing of the epitaxy substrate, depositing (col 11 ln 29) an electrically conductive, light-transmissive (transparent semiconductor: col 4 ln 64-65) window layer (117) over the device mesa and the second electrode, the window layer forming an electrical connection between the device mesa and the second electrode (col 8 ln 12-23).

Camras differs from the claimed invention only in not disclosing removing the epitaxy substrate after the flip-chip bonding.

Goosen is directed to flip-chip bonded GaAs-based light emitting diodes and teaches that it is frequently necessary to remove the GaAs substrate (col 1 ln 16-18), which is disclosed as a method comprising: flip-chip bonding (col 3 ln 9-11); after the flip-chip bonding, removing the substrate (col 3 ln 15-29); subsequent to the removing of the substrate, depositing a light-transmissive window layer (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Camras in view of Gooses such that the epitaxy substrate is removed after the flip-chip bonding; at least because this is a known suitable method achieving the desired purpose, and does not alter the resultant device function. See KSR v. Teleflex, 550 U.S. ___, 127 S. Ct. 1727 (2007).

RE claim 23, Camras discloses etching the epitaxy substrate (140) using one of wet chemical etching and plasma etching (col 11 ln 11-15).

RE claim 26, Camras discloses a method of manufacturing a light emitting diode (col 3 ln 55-60, col 4 ln 9-12), the method including (e.g., Figs 4 & 6, col 11 ln 21-24):

depositing a plurality of semiconductor layers (112, 114, 116) including group III-phosphide layers (col 4 ln 32-33) on a GaAs substrate (140, col 10 ln 39-40);

removing at least some of the deposited semiconductor layers from a selected trench region of the deposition substrate to define a light-emissive mesa (Fig 6D);

forming an electrode (118, col 11 ln 38) on the mesa (110 in Fig 5D);

flip-chip bonding (Fig 4, col 9 ln 30-32) the mesa to a first electrical bonding pad (134) of a thermally conductive (to any extent, as per MPEP § 2111) support (130);

removing the GaAs substrate (col 11 ln 27); and

subsequent to the removing of the GaAs substrate, depositing (col 11 ln 29) a light-transmissive, electrically conductive (transparent semiconductor: col 4 ln 64-65) window layer (117) on a surface of the mesa opposite the electrode.

Camras differs from the claimed invention only in not disclosing removing the epitaxy substrate after the flip-chip bonding.

Goosen is directed to flip-chip bonded GaAs-based light emitting diodes and teaches that it is frequently necessary to remove the GaAs substrate (col 1 ln 16-18), which is disclosed as a method comprising: flip-chip bonding (col 3 ln 9-11); after the flip-chip bonding, removing the substrate (col 3 ln 15-29); subsequent to the removing of the substrate, depositing a light-transmissive window layer (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Camras in view of Gooses such that the epitaxy substrate is removed after the flip-chip bonding; at least because this is a known suitable method achieving the desired purpose, and does not alter the resultant device function. See KSR v. Teleflex, 550 U.S. ___, 127 S. Ct. 1727 (2007).

RE claim 27, Camras discloses the deposited light-transmissive, electrically conductive window layer extends laterally to electrically contact a second electrical bonding pad (138) of the thermally conductive support to define an electrical path between the mesa and the second electrical bonding pad (col 8 ln 12-23).

RE claim 28, Camras discloses non-epitaxially depositing (encompassed by "conventional deposition techniques", col 10 ln 60-62) at least one window layer.

RE claim 29, Camras discloses depositing at least one GaP or AlGaAs window layer (col 4 ln 67, col 5 ln 1) by liquid phase epitaxy (LPE: col 10 ln 60-62).

RE claim 30, Camras discloses depositing said plurality of semiconductor layers by a deposition technique selected from the group consisting of metalorganic chemical vapor deposition and molecular beam epitaxy (col 10 ln 27-34, col 11 ln 23-26).

RE claim 31, Camras discloses non-epitaxially depositing (col 10 ln 40-46) at least one electrically conductive, light-transmissive window layer.

Response to Arguments

The arguments filed 01/28/2008 regarding Camras not teaching non-epitaxial deposition of the window layer have been fully considered but are not persuasive.

Camras anticipates this claim limitation in col 10 ln 40-46, even if one of skill in the art would not understand said limitation to be encompassed by "conventional".

The remaining arguments filed 01/28/2008 have considered, but are moot in view of the new grounds of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of time extension per 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For more info about PAIR, see http://pair-direct.uspto.gov. For questions PAIR access, contact the Electronic Business Center at 866-217-9197 (toll-free). For assistance from a USPTO Customer Service Rep or access to the automated info system, call 800-786-9199 or 571-272-1000.

/Andrew O. Arena/
Examiner, Art Unit 2811
2 April 2008

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811